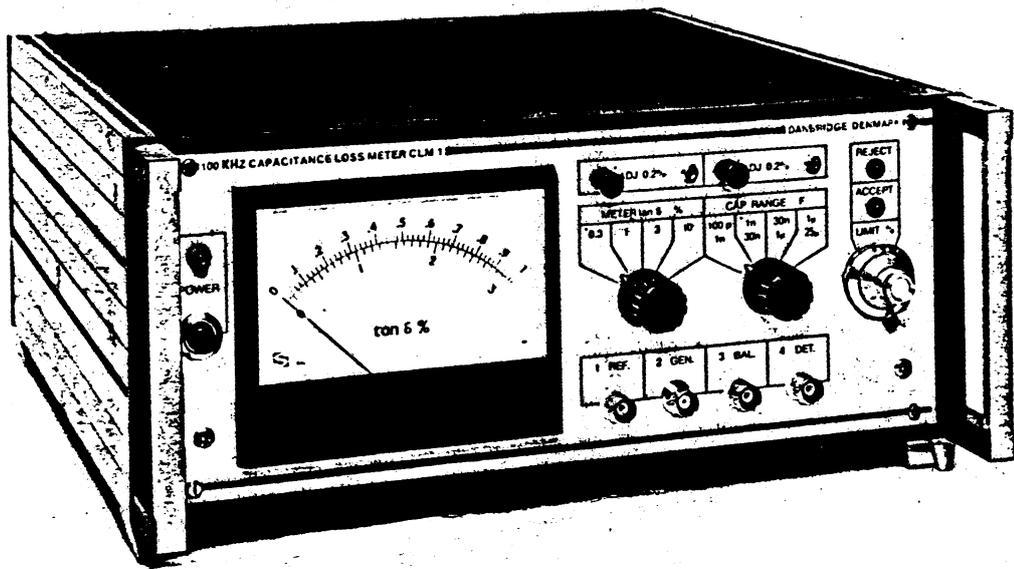


# INSTRUCTION MANUAL

DANBRIDGE  
DENMARK

## 100kHz Capacitance Loss-Meter CLM 1



SERIAL NO

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W A R N I N G

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The shields on the leads 2 and 3 should be connected together in the test jig.

They are grounded at just one point in the CLM 1 and should not be grounded anywhere else. The shields on test leads 1 and 4 must be isolated as they carry guard voltages.

If a shield is used at the test jig it can be connected to the shields of test leads 2 and 3 provided it is not connected to anything else.

## 1. INTRODUCTION

The CLM 1 is a four-terminal loss factor meter measuring  $\tan\delta$  directly in % at a measuring frequency of 100kHz.

The four-terminal arrangement eliminates measuring errors due to varying contact resistance in a test jig or an automatic sorting machine and makes it possible to measure  $\tan\delta$  with an accuracy of  $10^{-4}$ .

100kHz has been chosen as test frequency in order to perform accurate measurements of small variations of series resistance originating from differences in contact resistance between leads and foil. Losses due to contact resistance become more significant at 100kHz and can be measured with higher accuracy than with the standard test frequency of 1kHz.

The instrument is supplied in a cabinet with a width 2/3 of a 19 inch standard cabinet (a full 19 inch cabinet is optionally available) with a four-terminal test jig and a measuring cable from main frame to jig or test station fitted with BNC connectors.

The cable length is 1 meter allowing the CLM 1 to be connected to a sorting machine or to capacitors placed in a test chamber. Readout is provided on a panel meter and two analog outputs are available.

The instrument is supplied with a built-in analog limit comparator with a digital knob on the front panel for setting maximum  $\tan\delta$ . Green and red LEDs on the front panel indicate the ACCEPT/REJECT condition and a switch output is available.

## SPECIFICATIONS

Measuring frequency:	100kHz $\pm 0.1\%$
Capacitance range:	100pF - 25 $\mu$ F in four ranges 100pF - 1nF, 1nF - 30nF, 30nF - 1 $\mu$ F, and 1 $\mu$ F - 25 $\mu$ F
Tan $\delta$ accuracy:	100pF - 30nF: $1 \times 10^{-4}$ 30nF - 1 $\mu$ F: $3 \times 10^{-4}$ 1 $\mu$ F - 25 $\mu$ F: $3 \times 10^{-4} + C(\mu\text{F}) \times 10^{-4}$

Meter Display: Four ranges: 0.3, 1, 3, and 10%  
tan $\delta$  full scale.

Meter Display Accuracy:  $\pm 2\%$  reading  $\pm 1\%$  of full scale.

Measuring Voltage: Max. 1V rms.

Settling Time: Max. 50 milliseconds.

Analog Outputs:  $+10V$  for full scale meter deflection,  
 $-1V/\%$  absolute tan $\delta$ . (Min.  $2k\Omega$   
external load).

Terminals: Four-terminal connection with  
guard voltage on the shield of  
terminal 4.

Test Jig: Detector and generator terminal  
are 4mm jacks with 19mm spacing  
to enable the use of standard  
component fixtures.

Limit Output: Open collector (standard) rating  
 $35V/0.5A$  max. 3 watt. Cam relay  
(optional) with double shift-over  
contact rated  $220V/5A$  max. 500VA.

Power: 100-130V and 200-260V AC 50-60Hz,  
consumption 10VA.

Total Net Weight: 5.1kg

Dimensions: Height: 147mm  
Width: 325mm  
Depth: 356mm  
19" cabinet for rack mounting  
optional.

Accessories supplied: One pair of fixtures for axial-  
lead components.  
One fixture for radial-lead  
components.  
One power lead.

Accessories optional: Discharge Box DB1, for protecting  
the CLM 1 against charged capacitors.

## 2. OPERATING INSTRUCTIONS

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### 2.1. Setting Up

Check that the mains voltage selector is set to the actual supply voltage. The selector switch is located on the rear panel. Changing of the setting: Pull the knob, turn to the correct position and push back. Check that a 0.5A slow-blow fuse is fitted.

Connect the test jig or test station to the main frame with the measuring cable according to the number indications. Note that two sets of Generator/Reference terminals are provided on the test jig to enable measurements on capacitors of different lengths.

If a test station is used, please remember that the shield on terminal 4 is guarded and that the shield on terminal 1 must not be connected to earth on the test station. The shield on terminal 2, connected to the shield on terminal 3 in the test jig may be used as a ground connection from the main frame to test station.

As a four-terminal arrangement is used, the terminal 1 and 2 and the terminal 3 and 4 respectively must be interconnected before any checks or measurements are possible. When using the test jig and the test fixtures supplied by Danbridge, the terminals are automatically interconnected.

### 2.2. Initial Calibration

Set the Controls as follows:

Range Switch:	1nF-30nF
Meter Switch:	0.3% f.s.

Switch on the equipment and allow at least half an hour's stabilization before calibration.

Push the right push-button "ADJ. 0.2%" and adjust the corresponding potentiometer with a small screwdriver to 0.2% reading on the meter.

Push the left push-button "ADJ. 0.2%" and adjust the corresponding potentiometer to 0.2% reading on the meter.

When changing from the supplied test jig to a test station e.g. on a sorting machine it may be necessary to readjust the main frame (connected to the test station) as described in the "Maintenance Instructions" Section 4.2.

### 2.3. Measurements

Place the capacitor in the measuring jig. Set the range switch to the appropriate capacitance range and switch the meter switch to maximum reading within scale.

#### 2.3.1. Measurement Errors

When other test jigs than those supplied are connected to the terminals of the measuring cable, please keep in mind that the lead length between the terminals and the contacts should be as short as possible, and that additional ground capacitance should be avoided. These capacitances cause a measuring error, especially any capacitance to terminal 3 and 4. The error is largest on the 100pF-1nF range, e.g. with a 100pF in the test jig, 18pF between terminal 4 and ground gives about 0.025% low  $\tan\delta$  reading.

If the test jigs used do not provide any connection between terminals 3 and 4 with no measuring capacitor in circuit some drift may appear on the lowest ranges if the contacts are left open for more than a few seconds.

To eliminate this drift a resistor of about  $100\Omega$  may be connected between the terminals 3 and 4, as close as possible to the actual terminals.

#### 2.3.2. Analog Output

Two analog outputs are available at the rear output connector. One giving +10V for full scale meter deflection. This may be employed, e.g. for driving a remote meter or an external limit selector when high output at small values of  $\tan\delta$  is required. The second output is directly proportional to  $\tan\delta$  giving -1V for  $\tan\delta$  equal to 1% and may be employed to drive an external limit selector.

## 3. CIRCUIT DESCRIPTION

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### Diagrams 1 & 2

The Generator supplies the measuring voltage 1V rsm across the capacitor with unknown loss factor  $C_x$  in series with a standard resistor  $R_n$ . The voltages across  $C_x$  and  $R_n$ , the amplitude of which are a function of the capacitance of  $C_x$ , are feed into two phase-lock loop circuits PLL2 and PLL1 respectively.

The PLL circuits transform the sinusoidal signals into squarewaves with constant amplitude in precise phase-quadrature to the incoming signals. The squarewaves are fed into the Main Detector whose output is proportional to the phase difference between the squarewaves  $-90^\circ$ , i.e. proportional to  $\tan\delta$ .

The Main Detector output supplies  $-1V$  per % absolute  $\tan\delta$  for the Limit Comparator and the Meter Amplifier.

### 3.1. Details of Circuit

#### 3.1.1. The Measuring Circuit

Diagrams 3 & 4

The measuring voltage across  $C_x$  in series with  $R_n$  is supplied from the Generator via transformer L401. The junction between  $C_x$  and  $R_n$  is connected to the inverting input of an operational amplifier CA3030A, IC 403. The output of IC 403 is connected to the centre tap of the secondary of L401. This makes the input a virtual earth at zero potential which minimizes errors due to stray capacitance and cable capacitance from terminal 1 and 2 to ground. A current, taken from the output of IC 403 set by RV 403 and fed via R 411 into the inverting input of IC 403, compensates capacitive currents from terminal 4 to ground in order to eliminate errors at low value capacitor measurement.

In order to perform a true four-terminal measurement, the residual voltage at terminal 4 is fed to PLL2 via the voltage follower LM 310, IC 401. A guard voltage taken from the low impedance output of IC 401 is supplied via R 401 to the shield of the coax-cable to terminal 4, thus reducing the cable capacitance to ground.

In order to avoid errors at high value capacitor measurements due to cable inductance, the voltage at D is fed into PLL2 via the voltage follower LM 310, IC 402.

The standard resistors are mounted on a separate PC board on the Capacitance Range Switch.  $R_{N2}$ ,  $R_{N3}$ , and  $R_{N4}$  are separately shunted by an R-C network, compensating phase errors in the individual capacitance ranges due to shunt capacitance across the standard resistors.

It has been necessary to choose a value of  $R_{N1}$  lower than the optimum to ensure stability of the Measuring Circuit. This causes the voltage across  $R_{N1}$  for  $C_x < 400pF$  to be too low to ensure the prescribed phase stability of PLL1.

To overcome this problem the voltage across  $R_{N1}$  is amplified by the operational amplifier CA3030A, IC 404 before it is fed to PLL1, when the Range Switch is in position 100pF-1nF.

The Measuring Circuit has two built-in loss factor standards for adjustments. They are switched in between D and B with the adjust switches on the front panel, i.e. they are placed across the Detector and Generator Terminals of the test jig.

Each loss factor standard consists of one or more very low loss capacitors shunted by a resistor network adjusted to give a  $\tan\delta$  reading of 0.2% on the meter with the Range Switch in position 1nF-30nF.

### 3.1.2. The PLL Circuit

Diagrams 5, 6 & 7

The phase-lock loops PLL1 and PLL2 convert the sinusoidal voltages across  $R_N$  and  $C_X$  to squarewaves with 50% duty cycle, very small rise and fall times, constant amplitude and almost exactly in phasequadrature with the sinusoidal input signals.

PLL1 and PLL2 consists of a phase detector, a level shifter, a voltage-controlled oscillator and a flip-flop. As they are identical, only one, the PLL2 will be described in detail.

The phase detector is designed with the monolithic balanced modulator/detector MC1596, IC 201.

To bias it and enhance its performance the following circuits are added. A 12.1k $\Omega$  resistor R 215 to pin 5 sets the D.C. currents in the two branches to approx. 1.2mA. The lower differential inputs - the signal port - are biased with two resistor networks, one of them variable to balance the D.C. currents through the transistors.

The 3.16k $\Omega$  resistor R 213 between pin 2 and 3 (i.e. the emitters of the input transistors) sets the transadmittance of the signal stage.

The switching inputs are supplied with the squarewave outputs of the flip-flop IC 204.

The outputs (the crosscoupled collectors of the switching transistors) are current-feeding an operational amplifier IC 202, which adds gain and shifts the voltage level to an appropriate level for the control input of the voltage controlled oscillator (VCO).

The collector resistors R 214 and R 218 are matched to within 0.1% and to within 5ppm in temperature coefficient in order to reduce offset and temperature drift at the inputs of the amplifier. A balancing network is further applied to the collectors - R 216, R 217, and RV 202 - to increase common mode rejection. The potentiometer is set to keep the output of IC 203 constant when varying the current into pin 5 of IC 201 and thereby the D.C. currents through the device.

The 2.2 $\mu$ F capacitors, C 210 and C 211, decouple the A.C. components of the collector currents.

The levelshifter employs an integrated operation amplifier LM 725C, IC 202, because of its very low input offset voltage drift and input offset current, its high open loop gain and common mode rejections, and low input noise.

The amplifier is provided with an external offset null network by means of which it is possible to minimize the offset voltage drift. The R-C network in the feedback - and the similar one connected to the non-inverting input - sets the first pole and zero in the PLL loop, and sets the gain of the amplifier to approx.  $1V/\mu A$ .

The front-panel potentiometer RV 203 sets the voltage level at the output of the amplifier and hence the free-running frequency of the VCO, thus making it possible to adjust the phase error of the loop.

The output of the amplifier is fed to the control input of the VCO via R 229 and R 230 shunted by C 220. The junction point between R 220 and R 230 is clamped to the 5V supply voltage with the diodes D 201 and D 202. This limits the D.C.-control voltage to the VCO and ensures that the PLL is unable to lock on harmonics of the input frequency.

The VCO is a monolithic voltage-controlled oscillator XR 2207CP, IC 203 with excellent frequency stability. The free-running frequency is set by the polystyrene capacitor C 223 and the control voltage at pin 6 - the control input - to approx. 200kHz.

The voltage to frequency conversion gain  $K_o$  is controlled by C 223 and R 229 + R 230.

The squarewave output of IC 203 is fed to the clock input of the toggling flip-flop IC 204, which divides the VCO frequency by 2. The Q and  $\bar{Q}$  outputs of the flip-flop are fed back to the switching input of IC 201 through C 202 and C 201 thus closing the loop.

The flip-flop IC 204 is a schottky-clamped dual J-K flip-flop SN 74S113N. By setting the J, K, and preset inputs "high", the device forms a frequency divider. The squarewave outputs Q and  $\bar{Q}$  have exact 50% duty cycle and very small rise- and falltimes, which is necessary in order to minimize the effects of offset voltages on the switching inputs of - and the current imbalance in - the detectors.

### 3.1.3. The Main Detector

Diagram 8

The Main Detector consists of a phase detector and a level shifter. The phase detector is identical with the phase detectors in the PLL circuits described above, except for the gain setting resistor R 313 between pin 2 and 3.

The level shifter is designed with the operational amplifier LM 301A, IC 302. The R-C networks C 316 - R 326 and C 313 - R 325 set the gain of the level shifter and supply the output with the necessary noise suppression.

In addition they set the dominant pole of the total system, i.e. control the settling time.

RV 303 corrects the operational amplifier offset and hence the offset of the Main Detector.

#### 3.1.4. The Meter Amplifier

Diagram 9

The output of the Main Detector is applied to the Meter Switch, the four resistors of which control the gain of the operational amplifier LM 301A, IC 501. The output of IC 501 is fed to the  $\tan\delta$  Meter via RV 502 shunted by R 511 and R 512.

RV 502 sets the correct meter deflection - full scale for 10V at pin 6 of IC 501 - and D 501 connected between pin 6 and ground protects the meter against negative voltage excursions.

#### 3.1.5. The Generator

Diagram 10

The Generator consists of an oscillator and an output amplifier. It supplies the Measuring Circuit with a 100kHz 1V rms sinewave via transformer L 401. This sinewave must be very pure in order to avoid measuring errors due to odd harmonics. To achieve this a high-Q tuned circuit (Q about 300) is employed in the oscillator. This also ensures a good frequency stability determined mainly by the components of the tuned circuit.

The oscillator is designed with a tuned circuit and the transistor array CA 3054, IC 701 consisting of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate.

Only one of the amplifiers is used in a cascode configuration with positive feed-back.  $Q_2$ , one of the two common-base stages (formed by the differential pair  $Q_1$  and  $Q_2$ ) is used as a gain control.

The collector of  $Q_1$  feeds the tuned circuit - L 701 and C 708 - via a link (winding ratio 10:106) and another link (1 winding) delivers the positive feed-back signal to the base of  $Q_3$ .

The voltage of the tuned circuit is applied to the non-inverting input of operational amplifier LM 318, IC 702 which together with a push-pull stage constitutes the output amplifier. The output of IC 702 is supplied to the amplitude detector D 701, R 701, and C 701. The detector output is fed via RV 701 to the base of the gain control transistor  $Q_2$ . RV 701 sets the amplitude of the Generator output signal. IC 702 feeds the push-pull stage formed by  $Q_702$  and  $Q_703$  and biased by  $Q_701$ . The push-pull output voltage is fed back to the inverting input of IC 702 via the resistive divider R 707 and R 706 in order to minimize the total harmonic distortion of the output amplifier.

The output amplifier is able to deliver 1V rms/500mA via the transformer L 401 (see diagram 3) to the Measuring Circuit.

### 3.1.6. The Limit Comparator

Diagram 11

A voltage proportional to  $\tan\delta$  supplied from the Main Detector is fed into the non-inverting input of operational amplifier LM 301A, IC 601. IC 601 is connected as a voltage comparator. A small amount of hysteresis ( approx. 7mV  $\tan\delta$  equal to 0.007%) is provided by positive feed-back from the output via R 605 to the non-inverting input. R 601 in series with the front-panel mounted 10-turn potentiometer RV 601 connected between -15V and ground form a voltage divider. The voltage level at the arm of RV 601 is fed via R 603 to the inverting input of IC 601 as a reference voltage. The digital knob mounted on RV 601 sets the maximum value of  $\tan\delta$ .

The output of IC 601 feeds the base of the LED-driver transistor Q 601 and the output darlington transistor Q 602. The collector of R 602 is connected to pin 5 at the rear panel socket.

When the Main Detector output is more positive than the reference voltage, i.e. when  $\tan\delta$  is lower than the preset value, the output of IC 601 goes "high" and the collectors of Q 601 and Q 602 go "low" turning on the green LED 601 mounted on the front panel. The voltage level at the junction point K between R 608 and LED 601, which feeds the base of LED-driver Q 603 via R 609 goes "low" cutting Q 603 off.

When the Main Detector output is more negative than the reference voltage, i.e. when  $\tan\delta$  is higher than the preset value, the output of IC 601 goes "low" and the collectors of Q 601 and Q 602 go "high". Q 603 saturates and the red front-panel mounted LED 602 switches on.

A cam relay with double shift-over contacts (rated 220V/5A max. 500VA) is optionally available. The CLM 1 is prewired for the cam relay (Siemens V23154 D0717-F104) and the relay socket is mounted as standard.

N.B.: When the cam relay is mounted, loads connected between the open collector output at pin 5 and supply voltages lower than +15V may cause malfunction of the relay.

### 3.1.7. The Power Supply

Diagram 12

The regulators for the power supply voltages ( $\pm 15V$  and  $+5V$ ) are placed on two PC boards mounted on the rear panel together with the power transformer, the line voltage selector, the fuse, and the line voltage input socket.

The  $\pm 15V$  supply is designed with an integrated dual-voltage regulator driving the two power transistors MJE 3055 and MJE 2955, which use the rear panel as heatsink. Two potentiometers control the output voltage values and balance respectively.

The +5V supply is independent of the  $\pm 15V$  supply and designed with the integrated regulator LM 723 driving the MJE 2955 output transistor. A potentiometer for precise output voltage setting is provided.

#### 4. MAINTENANCE INSTRUCTIONS

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The adjustments by the two front-panel controls - as described in the Operation Instructions - should suffice for a trouble-free long term use. If a test station or test jig with longer leads than those supplied with the test jigs is used, or if a degrading of the measuring accuracy appears, which cannot be countered by the front-panel adjustments, a realignment of the factory-set potentiometers inside the apparatus may be necessary as described in section 4.2.

In case of repair, a realignment of the individual circuits may be necessary as described in section 4.1., followed by a realignment of the whole system as described in section 4.2.

##### THE USER IS WARNED:

Follow the instruction manual carefully and do not replace the matched resistors (R 114, R 118, and R 214, R 218) or the balanced modulators MC 1596 (IC 101 and IC 201) in the PLL circuits by others than the appropriate spare parts delivered by Danbridge

If an adjustment is made it is necessary to use a digital voltmeter (DVM), an amplifying AC-voltmeter (AVM), a frequency counter, an oscilloscope with a high impedance probe, and six capacitors with known very small loss factors at 100kHz ( $\tan\delta < 0.1\%$ ) and values of 100pF, 1nF, 5.6nF, 30nF, 1 $\mu$ F, and a 15-20 $\mu$ F.

In order to obtain easy access to the PC boards loosen the four screws in each corner of the front panel and pull the main frame out from the cabinet.

#### 4.1. Alignment of Individual Circuits

##### 4.1.1. Supply Voltage Adjustment

The  $\pm 15V$  supply on PC board 89207, mounted on the rear panel, is adjustable with two single-turn potentiometers. The right-hand potentiometer (seen from the upper side) sets the positive voltage, and the left-hand potentiometer sets the balance. The +15V and the -15V should not deviate more than a few millivolts from the nominal values.

The +5V supply on PC board 89216A, mounted on the rear panel, is set to +5.10V by  $1k\Omega$  single-turn potentiometer in order to supply the correct clamp-voltage to the PLL circuits.

#### 4.1.2. Adjustment of the PLL Circuits

As PLL1 and PLL2 are identical, only the adjustment of PLL2 will be described.

If the measuring cable and the test jig with its test fixtures are disconnected, then connect on the main frame terminal 1 to terminal 2 and terminal 3 to terminal 4 with coax-cables.

Remove IC 701 from the Generator to secure that no signal is applied to the signal port of the phase detector IC 201.

Disconnect the filter capacitor C 211 from IC 201 pin 9 to ground by means of the print switch SW 201, and short the switching output of IC 201 (pin 6 to pin 9).

Measure  $V_{iO}$ , the voltage difference between IC 202 pin 6 and the arm of RV 203 (the junction point between R 224 and C 212), with the DVM and adjust RV 204 to Zero  $V_{iO}$  reading.

Remove the short from the switching output and connect a counter (or oscilloscope) to IC 204 pin 1.

Adjust the left "ADJ. 0.2%" potentiometer on the front panel to 200kHz counter reading (within  $\pm 2\%$ ).

Connect the oscilloscope to IC 201 pin 9 and observe the squarewave feedthrough. Adjust RV 201 to minimum feedthrough.

Reconnect the filter capacitor C 211.

The balancing network applied to the switching output of IC 201 (R 216, R 217, and RV 202) must be adjusted to keep the output constant when the current into pin 5 is varied and thereby the DC current through the device. This is carried out as follows: Connect the DVM to the output of IC 202 (pin 6). Observe the DVM reading. Shunt R 215 with a  $100k\Omega$  resistor and observe the DVM reading. Adjust RV 202 to the same reading with and without the  $100k\Omega$  shunt.

#### 4.1.3. Adjustment of the Main Detector

Insert IC 701 in the Generator and check the Generator frequency ( $100kHz \pm 0.1\%$ ).

Remove IC 203 from PLL2 and disconnect the filter capacitor C 312 from IC 301 pin 9 to ground by means of the print switch SW 301.

Connect the oscilloscope to IC 301 pin 9 and observe the carrier feedthrough. Adjust RV 301 to carrier null. Connect the filter capacitor C 312.

The adjustment of the balancing network applied to the switching output of IC 301 (R 316, R 317, and RV 302) is carried out by using the same procedure as in the PLL circuits (see above).

#### 4.1.4. Adjustment of the Generator

Connect the counter to the Generator output (the junction point between R 712 and R 713). Adjust the frequency to 100.00kHz with the inductance adjustor in the oscillator coil.

Connect the AVM to the Generator output and adjust the output amplitude to 7V rms with the amplitude control potentiometer RV 701.

#### 4.1.5. Adjustment of the Meter Amplifier and the Limit Comparator

Set the controls as follows:

Range Switch:	1nF-30nF
Meter Switch:	1% f.s.

Connect the DVM to the Main Detector output (the rear panel socket pin 3). Push one of the "ADJ. 0.2%" switches and observe the DVM reading.

Connect the DVM to the Meter Amplifier output (the rear panel socket pin 4). Push the switch again and adjust RV 501 until the DVM shows -10 times the previous DVM reading.

Switch the Meter Switch to 0.3% f.s. With the DVM connected to the rear panel socket pin 4, push one of the "ADJ. 0.2%" switches, set RV 303 (in the Main Detector) to 9.49V DVM reading, and adjust RV 502 to 0.3%  $\tan\delta$  Meter reading.

#### 4.2. Alignment of Measuring Circuit and the Complete System

Connect the test jig or test station to be used to the main frame via the Measuring Cable and set the controls as follows:

Range Switch:	1nF-30nF
Meter Switch:	0.3% f.s.

- a. Mount the 5.6nF capacitor  $C_1$  in the test jig. Offset the Main Detector output to 0.1% meter reading with the offset potentiometer RV 303 (in the Main Detector).

Mount the  $1nF$  capacitor  $C_2$  in the test jig. Adjust the right "ADJ. 0.2%" potentiometer RV 103 on the front panel (With a screwdriver) until the correct loss factor appears on the meter when switching from  $C_1$  to  $C_2$ .

EXAMPLE: Let the loss factor of  $C_1$  be 0.03% and the loss factor of  $C_2$  be 0.01%. Then the correct adjustment of R 103 would cause a difference between the two meter readings of -0.02%, when  $C_1$  is replaced by  $C_2$  in the test jig.

- b. Mount  $C_1$  in the test jig and reset RV 303 to 0.1% meter reading. Replace  $C_1$  by the  $30nF$  capacitor  $C_3$ . Adjust the left "ADJ. 0.2%" potentiometer RV 203 until the correct loss factor difference appears on the meter when switching from  $C_1$  to  $C_3$ .

Repeat point a. and b. until correct loss difference appears on the meter in both cases.

- c. Switch the Range Switch to  $100pF-1nF$ . Mount  $C_2$  in the test jig and adjust RV 303 for 0.1% meter reading.

Replace  $C_2$  by the  $100pF$  capacitor  $C_4$ . Adjust RV 403 until the correct loss difference appears on the meter when switching from  $C_2$  to  $C_4$ .

If more than a very small adjustment ( $2-3 \times 10^{-4}$ ) is necessary repeat a., b., and c.

Mount  $C_2$  in the test jig. Switch the Range Switch to  $1nF-30nF$  and observe the meter reading. Switch the Range Switch to  $100pF-1nF$ . Adjust C 412 for identical meter readings.

Switch the Range Switch to  $1nF-30nF$ . Mount  $C_3$  in the test jig and observe the meter reading. Switch the Range Switch to  $30nF-1\mu F$ . Adjust RV 802 (the left-hand potentiometer on the standard resistor PC board) for identical readings.

Mount a  $1\mu F$  capacitor (use a polycarbonate capacitor with a small loss factor for highest accuracy) in the test jig.

Switch the Meter Switch to the appropriate range and observe the meter reading. Switch the Range Switch to  $1\mu F-25\mu F$ .

Adjust RV 803 (the right-hand potentiometer on the standard resistor PC board) for identical readings.

Set the Range Switch in position  $1nF-30nF$  and the Meter Switch to position 0.3% f.s. Mount  $C_1$  in the test jig and adjust RV 303 (in the Main Detector) for the correct meter reading (the correct absolute value of  $\tan\delta$ ).

Remove  $C_1$  from the test jig and make sure that terminal 1 is shorted to terminal 2 and terminal 3 shorted to terminal 4 by the test fixtures.

Push the right-hand "ADJ. 0.2%" bush-button and adjust RV 401 (mounted on the main PC board) to 0.2% meter reading.

Push the left-hand "ADJ. 0.2%" push-button and adjust RV 402 to 0.2% meter reading.

#### 4.2.1. Adjustment procedure in the $1\mu\text{F}$ - $25\mu\text{F}$ range

Necessary standards:

$C_4$ :  $1\mu\text{F}$ ,  $\tan\delta \leq 2 \times 10^{-3}$  accuracy  $1 \times 10^{-4}$

$C_5$ :  $15$ - $20\mu\text{F}$ ,  $\tan\delta$  approximately 1-3% accuracy  $5 \times 10^{-4}$

Adjust the ranges  $100\text{pF}$ - $1\text{nF}$ ,  $1\text{nF}$ - $30\text{nF}$ , and  $30\text{nF}$ - $1\mu\text{F}$  as described above.

1. Place  $C_4$  in the test jig.  
Range switch in  $30\text{nF}$ - $1\mu\text{F}$  range. Adjust RV 404 for correct reading.  
(NOTE: If adjustment range is too small, change R 423).
2. Range switch to  $1\mu\text{F}$ - $25\mu\text{F}$ . Adjust RV 803 to same reading.
3. Place  $C_5$  in test jig.  
If the reading deviates from the correct value with more than the stated tolerance (see page 1) change R 427.  
NOTE: If R 427 is changed the whole Measuring Circuit must be readjusted and the above pont 1-3. (Remember also to adjust the two "ADJ. 0.2" potentiometers RV 401/402).

#### 4.3. Check points and check procedure in case of repair

Remove the top cover of the instrument.

Connect the test jig to the main frame via the measuring cable. Mount a  $33\text{nF}$  or a  $27\text{nF}$  capacitor in test fixture and set the controls as follows:

Range Switch:	$1\text{nF}$ - $30\text{nF}$
Meter Switch:	10% f.s.

Switch on power.

1. Check the Power Supply (in the rear end of the Main PC board).
2. Check the Generator output (TP2 in the Generator circuit). Pure sin. wave., frequency 100.00kHz, amplitude 7V rms.
3. Check that PLL2 is locked on the Generator frequency. Use a 2-channel oscilloscope: Display mode alternating, trigger source CH1. Connect CH1 to TP2 in the Generator and CH2 to TP2 (or TP3) in PLL1 and PLL2 via a 10:1 probe.

If the display shows a 3Vpp squarewave and no movement with respect to the Generator signal, the PLL's are locked.

4. Check with the oscilloscope that the PLL output signal appears on the Main Detector: 3Vpp squarewave - pin 1 and pin 4, IC 301 300mVpp squarewave pin 7 and pin 8, IC 301.
5. Check the measuring circuit with the oscilloscope (use a 10:1 probe).

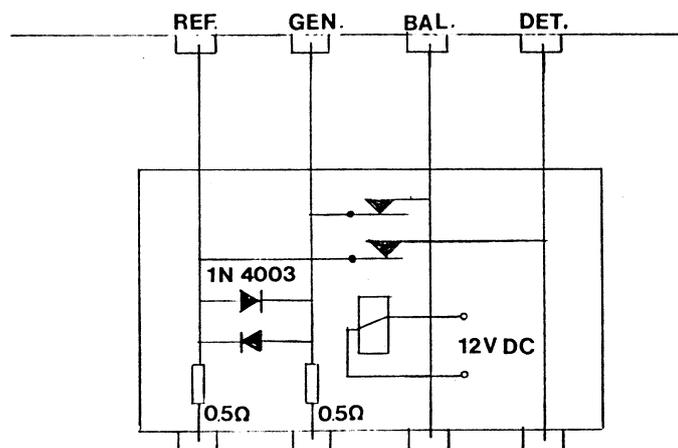
TP1: 1V rms sin.wave.  
 TP2: ~4V rms sin.wave.  
 TP3: ≤5mVpp sin.wave. (if >5mV check IC 403).  
 TP4: ≤5mVpp sin.wave.  
 TP5: 0.2V rms sin.wave.

6. Check output of the Main Detector. Connect the oscilloscope to TP2 in Main Detector circuit. If the output noise is >10mVpp, check PLL2. Change the Range Switch to 30nF-1μF. If the output noise is >10mVpp, check PLL1.

If one of the individual circuits fails, check the bias voltage and try to readjust the circuit (see Maintenance Instructions).

5. Discharge Box, type DB 1

RELAY: SIEMENS 23154 D0 717 F104  
(OR EQUIVALENT)



The DB 1 discharge box is intended for use with the CLM 1 in applications where capacitors with potentially damaging DC charges may reach the measuring jig.

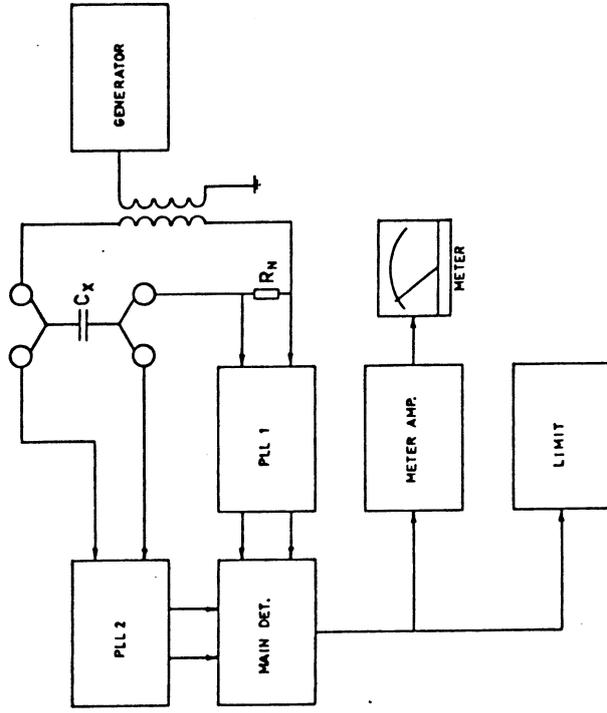
The CLM 1 is guaranteed to withstand discharge of 30V. It is not possible to increase this limit significantly without decreasing the sensitivity and thereby the accuracy of the instrument.

It is strongly recommended to discharge the capacitors thoroughly before applying them to the measuring jig. If total discharge cannot be guaranteed the DB 1 may be used to further decrease the probability of damage to the CLM 1.

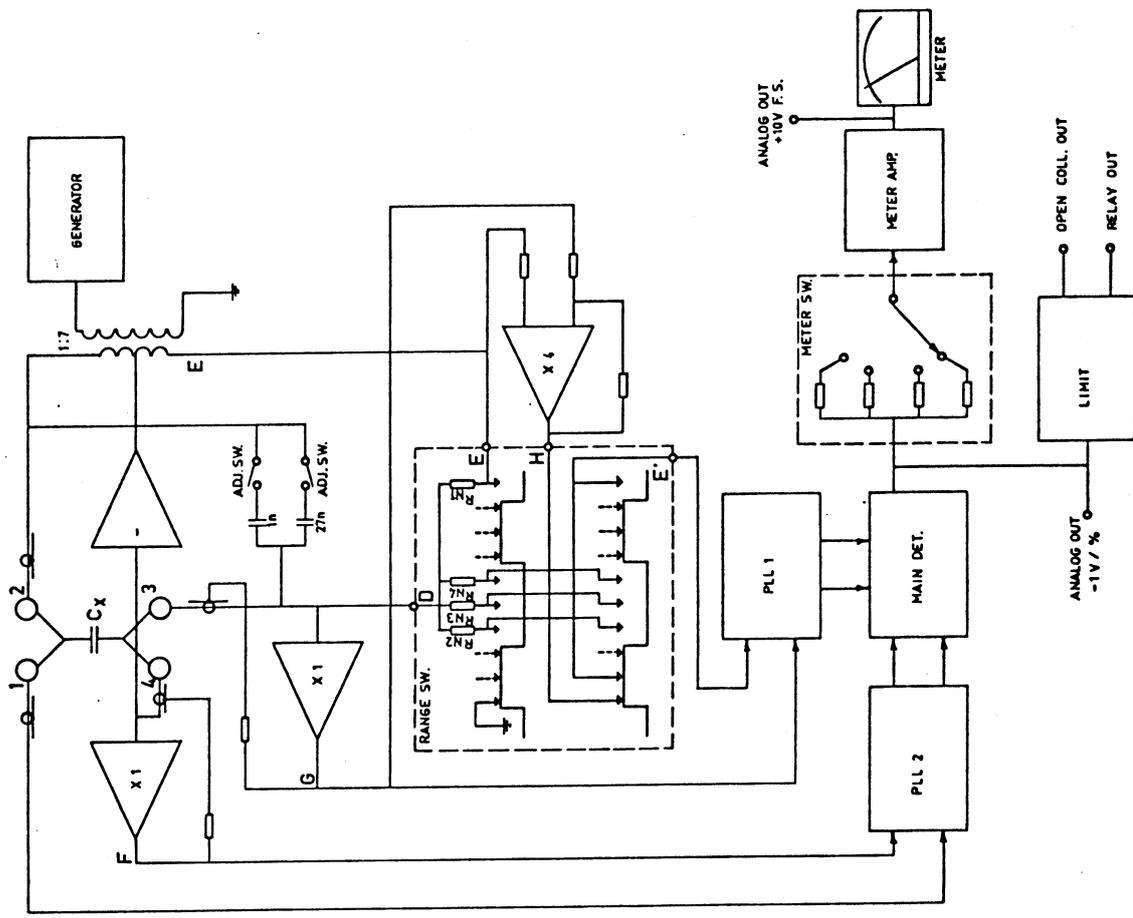
The DB 1 is inserted between the jig and the CLM 1 and its relay breakcontacts keeps the jig shorted until the relay is activated by the user. The relay needs an external 12V supply to operate.

The relay should be inserted and/or replaced periodically if repeated high voltage discharging are experienced or suspected, owing to the possible degrading of the contacts.

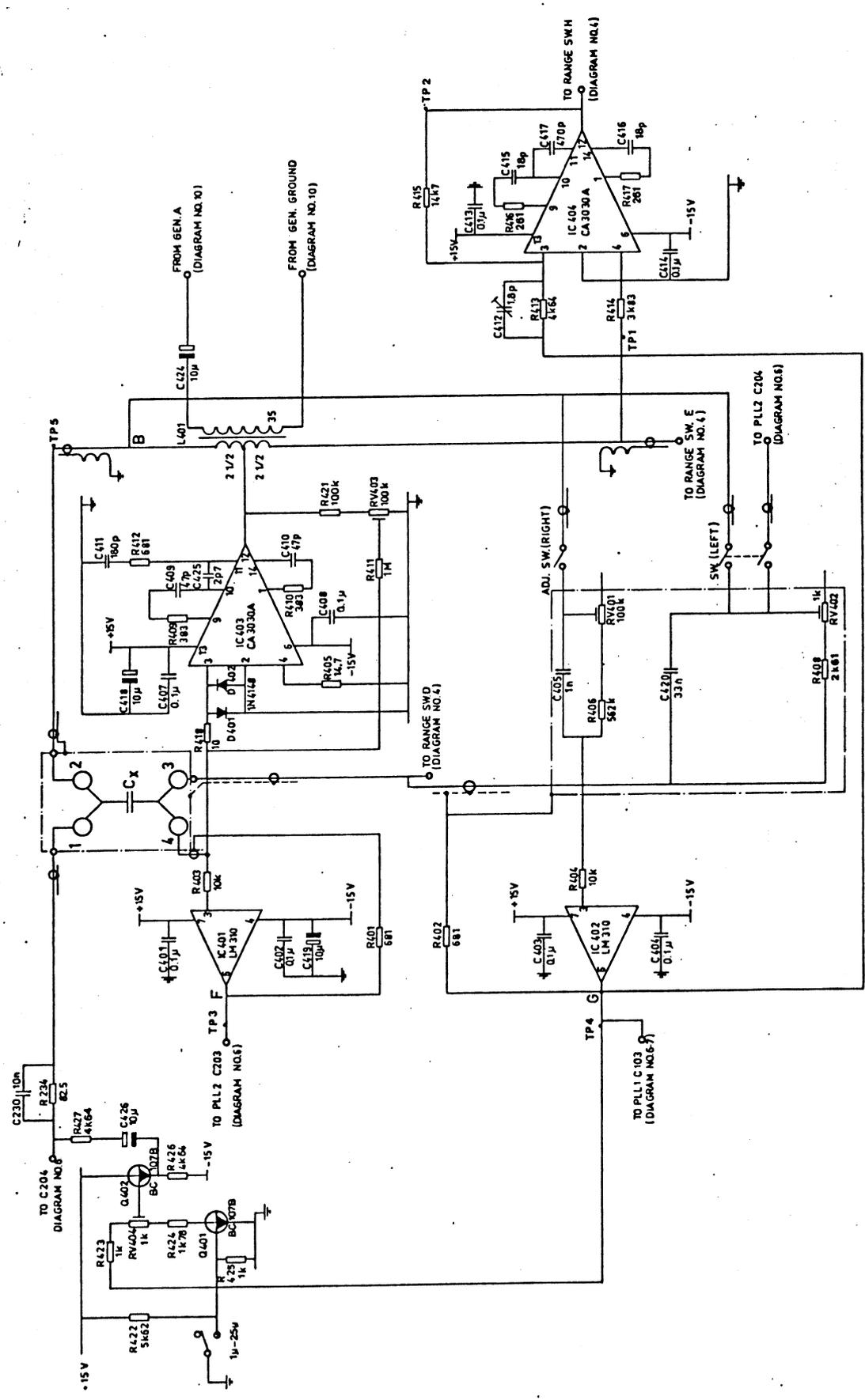
The CLM 1 must be recalibrated using the procedure described in section 4.2. when the DB 1 is applied.



72550-1	CLM1 DIAGRAM NO.1						
A/S DANBRIDGE	SIMPLIFIED			RETTET	GDDK.		
	BLOCK DIAGRAM			TEGNET:	110376 B. Res.		
				KONSTRUERET:	S. KOFED OLFSEN		
				BODKENDT:			14

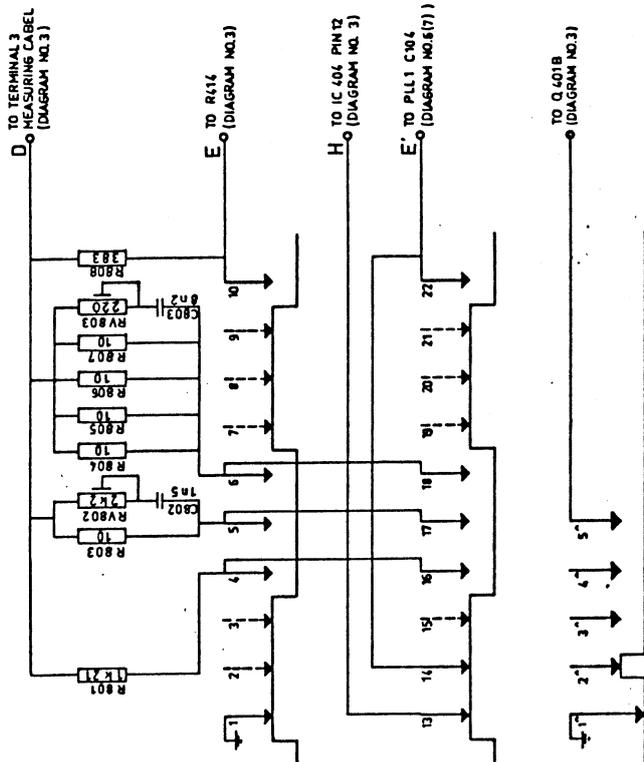


72550-2	CLM 1 DIAGRAM NO.2		
A/S DANBRIDGE	BLOCK DIAGRAM		
	RETTET	600K.	
	TEGNET:	120376 B. Pnl.	
	KONSTRUERET:	S. KORFED OLSEN.	
	Godkendt:		15



72550-3	CLM1 DIAGRAM NO.3	291276 BR	PL	010278BR	
A/S DANBRIDGE	MEASURING CIRCUIT	210876 BR	PL	170778 BR	
		RETTET	GOODK.	180376 BR	
		TEGNET		S. HOFDEED OLSEN	
		KONSTRUERET:		GOODKENDT:	

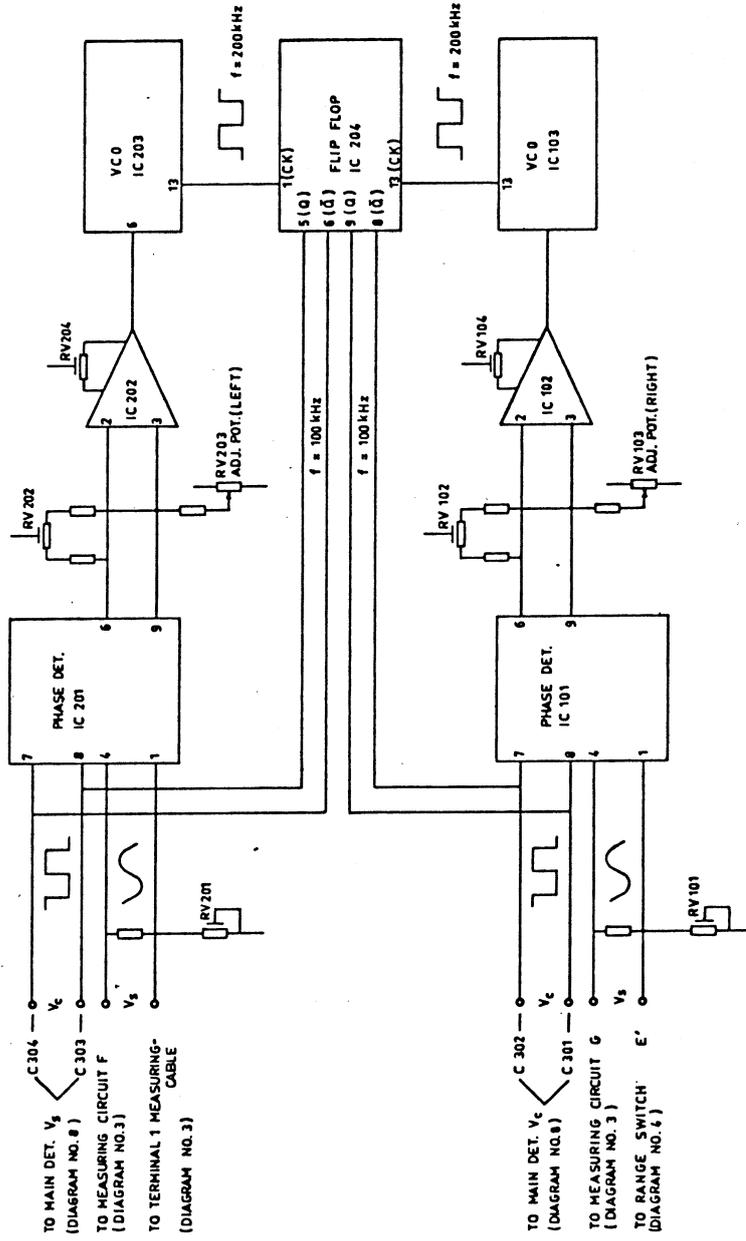
CAP RANGE F



RANGE

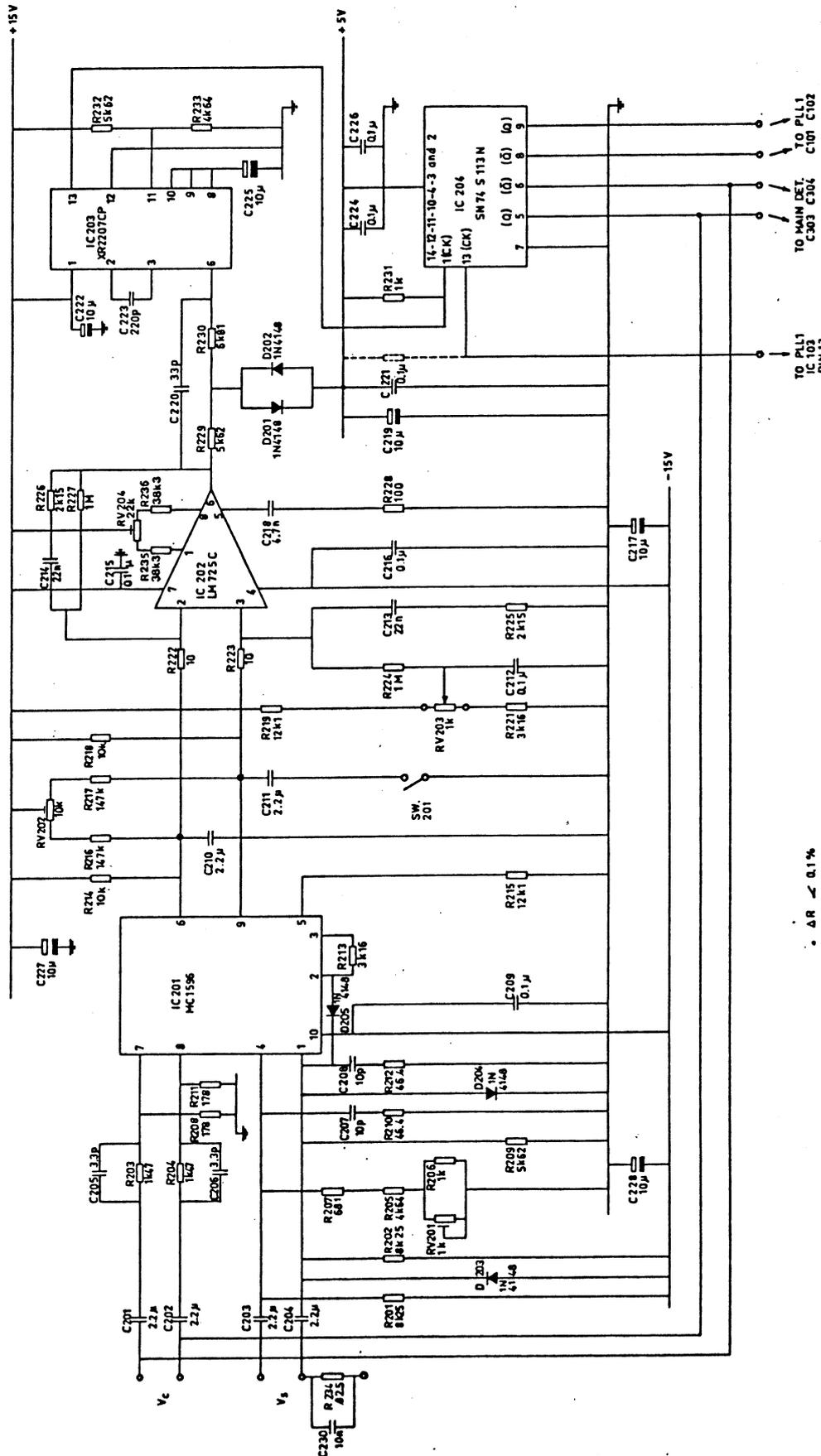
100p - 1n	R <sub>N1</sub>	R 808	= 383 Ω
1n - 20n	R <sub>N2</sub>	R808 # R801	= 291 Ω
20n - 1 μ	R <sub>N3</sub>	R <sub>N1</sub> # R803	= 966n
1 μ - 25 μ	R <sub>N4</sub>	R <sub>N1</sub> # R804 # R805 # R806 # R807	= 2.00μ

72550-4	CLM1 DIAGRAM NO. 4			
	RANGE SWITCH			
	A/S DANBRIDGE			
	170778 BR	1/4		
0702778	1/4			
RETTET	GOODK	070278BR	1/4	
TESNET				
MONSTRUERET I			S. HOFJED OLSEN.	
GOODKENDT			1/4	



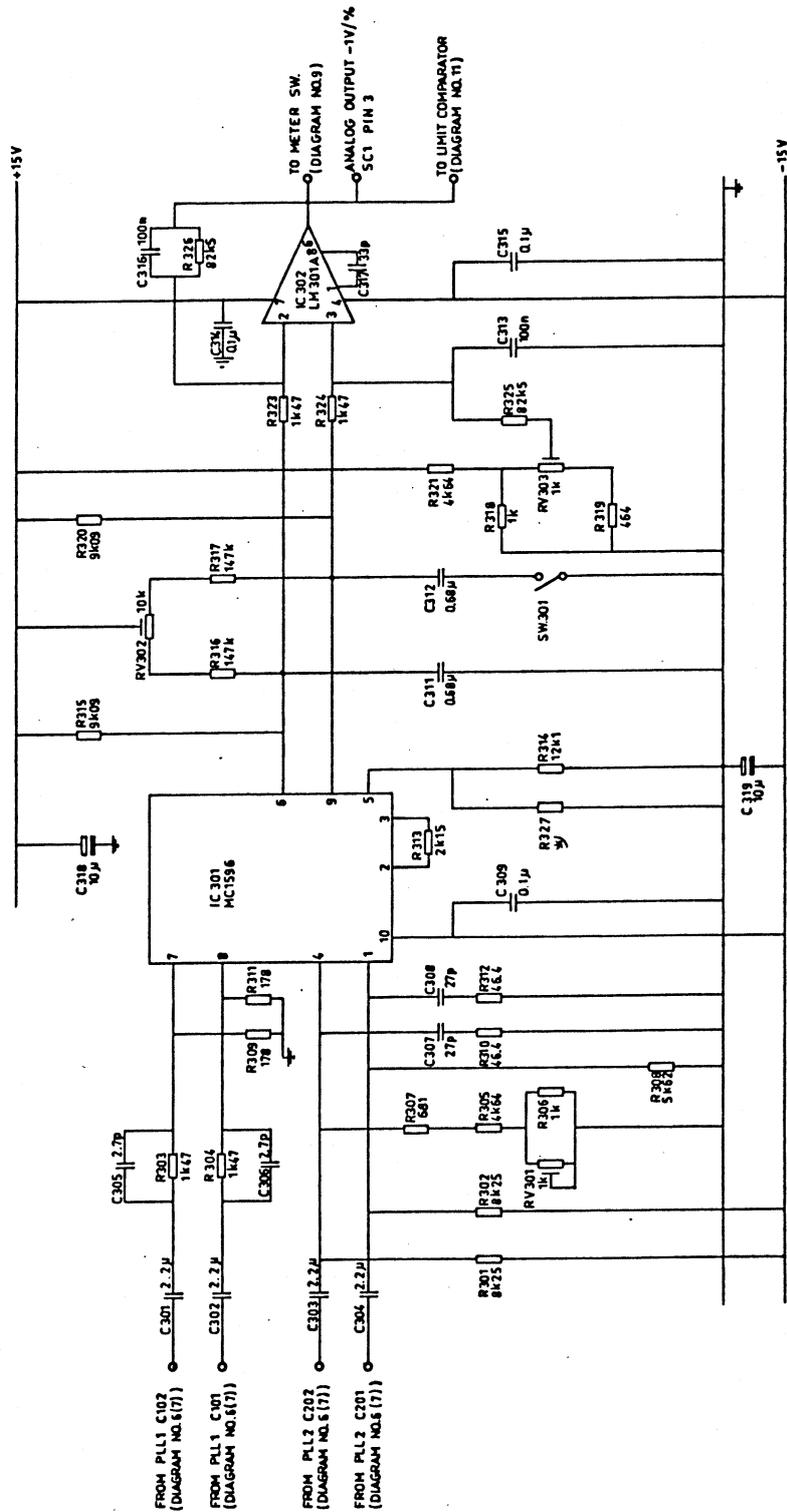
RV 103 and RV 203 is front panel multivibrator potentiometers.

72550-5		CLM1 DIAGRAM NO.5	
A/S DANBRIDGE		PLL SYSTEM	
BLOCK DIAGRAM			
RETIET	GDDK		
TEGNET	300376 R.ROS.		
KONSTRUERET	S. KOPPEL OLSEN		
GODKENDT	JL		



FOR PL11 REPLACE #22# WITH #11# EXCEPT FOR IC204 - C224 AND C226 WHICH ARE IN COMMON.

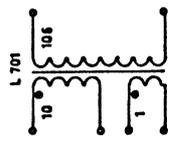
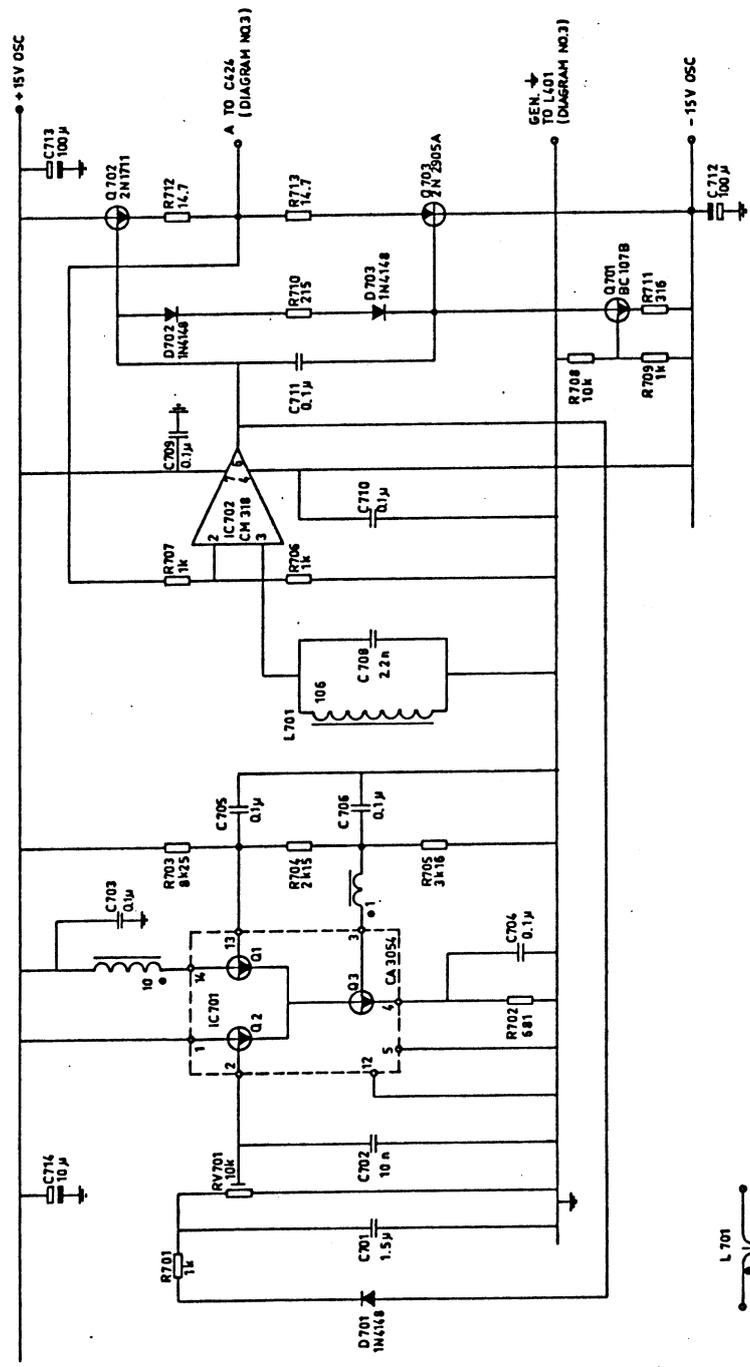
72550-6(7)	CLM 1 DIAGRAM NO.6(7)
A/S DANBRIDGE	PHASE LOCK LOOP 2.(8.1)
180778 B.R.	1/5
231276 B.R.	1/5
RETTET	GODK.
TEGNET.	50676 B.ROT.
MONSTRUERET.	S. KROGED OLTEN.
6000.	7/5



RV303 ADJUSTS THE MAIN DETECTOR GAIN

72550-8	CLM1 DIAGRAM NO. 8			
A/S DANBRIDGE	MAIN DETECTOR			
	190778 BR	SL		
	119227 BR	SL		
	RETTET	GOODK.	120379 BR	SL
	TEGNET		810176 B. Rgt.	
	MONSTRUERET:		S. HOFDZED OLSEN	
	GOODK.			

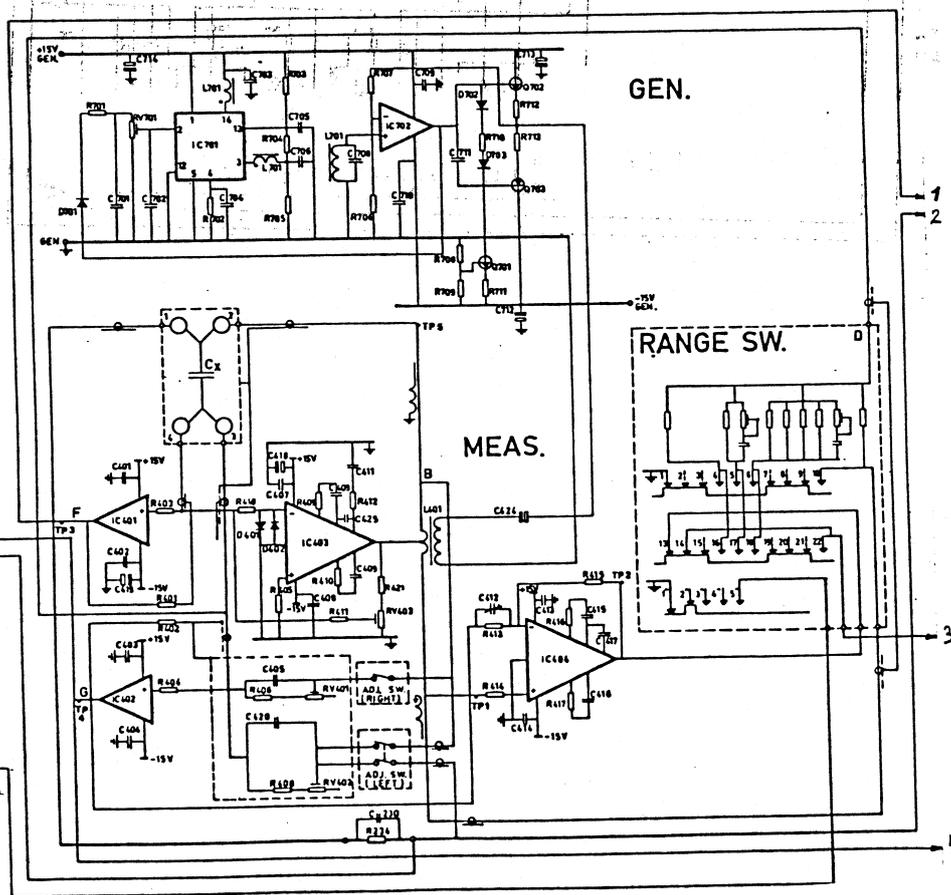




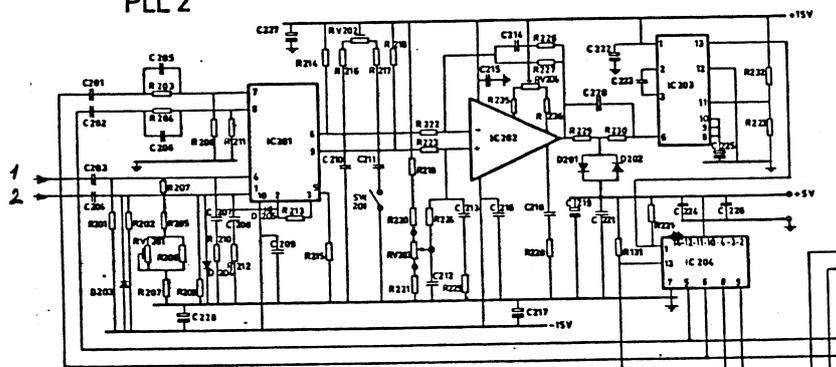
72550 - 10	CLM 1 DIAGRAM NO.10	021078 BR	
A/S DANBRIDGE	GENERATOR	190779 BR	15
		RETTET	GDDK.
		TEGNET	
		KONSTRUERET:	S. KOPPEL OLSSEN.
		GDDK.1	



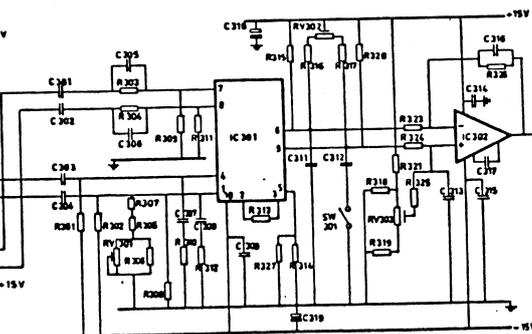




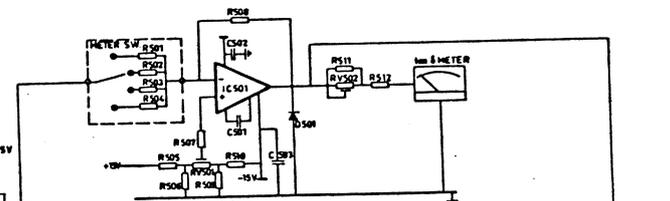
PLL 2



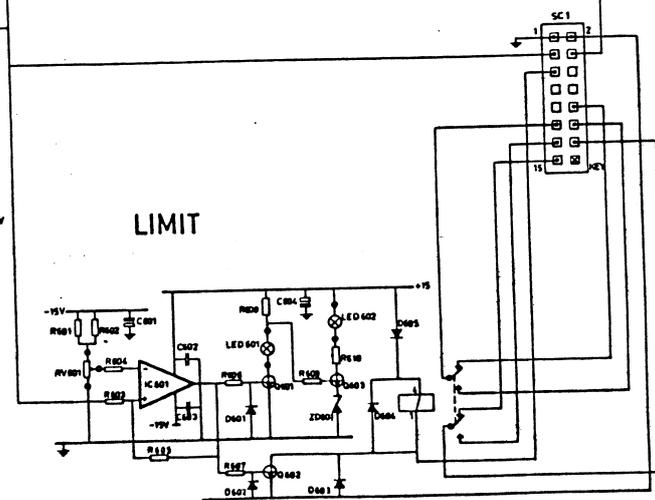
MAIN DET.



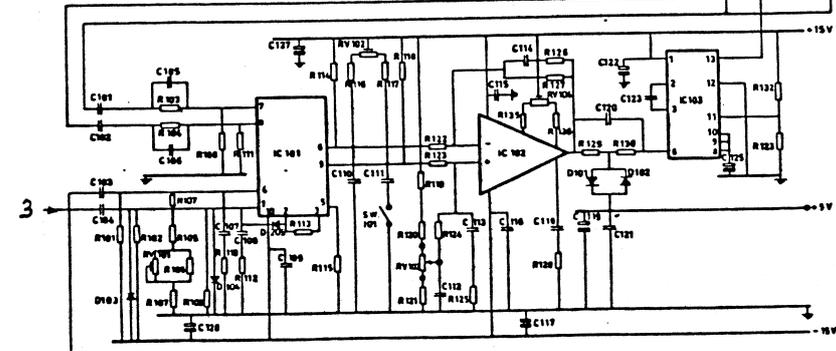
METER AMP.



LIMIT



PLL 1

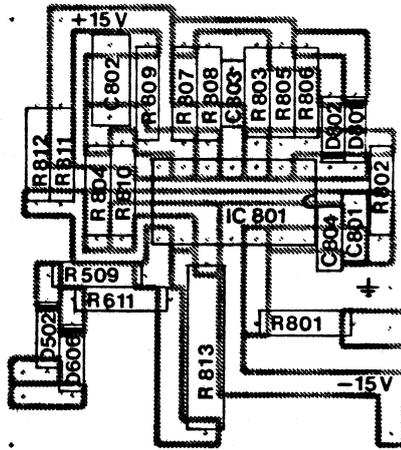


CLM 1

72550-13 A/S DANBRIDGE.	DIAGRAM NO.13		10078000	22027500
	ELECTRONICS		REVISED	REVISED
			110376	0 Rev.
			CONTRIBUTOR:	CONTRIBUTOR:

# CIRCUIT BOARD OCD-CLM 1

1 MJC-000



OPEN CIRCUIT DETECTOR

